

Application Serial No. 10/738,397
Reply to office action of November 30, 2006

PATENT
Docket: CU-3496

Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (previously presented) A method for fabricating a semiconductor device, which comprises the steps of:
 - forming a gate line on a semiconductor substrate;
 - forming successively a buffer layer, a spacer nitride film, and a spacer oxide film on the entire surface of the substrate including the gate line;
 - selectively etching the buffer layer and the spacer nitride film in such a manner that they remain on both sides of the gate line;
 - performing an ion implantation process using the remaining buffer layer and spacer nitride film as a barrier film to form junction regions in the semiconductor substrate at both sides of the gate line;
 - subjecting the entire upper portion of the substrate including the junction regions to a rapid thermal annealing (RTA) process;
 - forming an interlayer insulating film on the entire upper portion of the resulting substrate;
 - selectively removing the interlayer insulating film to form contact holes exposing the upper surface of the junction regions; and
 - forming contact plugs in the contact holes.
2. (canceled)

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3. (previously presented) The method of claim 1, wherein the buffer layer is in the form of a laminated structure of an oxide film and a nitride film, a single-layered oxide film, or a single-layered nitride film.
4. (previously presented) The method of claim 1, wherein the spacer nitride film is formed to a thickness of 100-700 Å.
5. (previously presented) The method of claim 1, wherein the ion implantation process is performed using a given tilt angle and a given number of rotations.
6. (original) The method of claim 5, wherein the tilt angle is 0 to 30° and the number of rotations is 2 to 4.
7. (canceled)
8. (original) The method of claim 1, which additionally comprises the step of performing a rapid thermal annealing (RTA) process after the step of forming the interlayer insulating film.
9. (original) The method of claim 1, which additionally comprises the step of subjecting the interlayer insulating film to a reflow annealing process and a rapid thermal annealing process after the step of forming the interlayer insulating film.

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10. (original) The method of claim 1, which additionally comprises the step of performing a high temperature rapid thermal annealing process before forming the contact plugs, and the step of a low temperature rapid thermal annealing process after forming the contact plugs.

11. (previously presented) The method of any of claim 8, wherein the buffer layer is in the form of a laminated structure of an oxide film and a nitride film, a single-layered oxide film, or a single-layered nitride film.

12. (previously presented) The method of any of claim 8, wherein the spacer nitride film is formed to a thickness of more than 90 Å.

13. (previously presented) The method of any of claim 8, wherein the ion implantation process is performed using a given tilt angle and a given number of rotations.

14. (original) The method of claim 13, wherein the tilt angle is 0 to 30° and the number of rotations is 2 to 4.

15. (canceled)

16. (previously presented) The method of Claim 9, wherein the buffer layer is in the

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form of a laminated structure of an oxide film and a nitride film, a single-layered oxide film, or a single-layered nitride film.

17. (previously presented) The method of claim 9, wherein the sapacer nitride film is formed to a thickness of more than 90 Å.

18. (previously presented) The method of Claim 9, wherein the ion implantation process is performed using a given tilt angle and given number of rotations.

19. (previously presented) The method of claim 18, wherein the tilt angle is 0 to 30 ° and the number of rotations is 2 to 4.

20. (previously presented) The method of claim 10, wherein the buffer layer is in the form of a laminated structure of an oxide film and a nitride film, a single-layered oxide film, or a single-layered nitride film.

21. (previously presented) The method of claim 10, wherein the spacer nitride film is formed to a thickness of more than 90 Å.

22. (previously presented) The method of claim 10, wherein the ion implantation process is performed using a given tilt angle and a given number of rotations.

23. (previously presented) The method of claim 22, wherein the tilt angle is 0 to 30 °

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and the number of rotations is 2 to 4.

24. (new) The method of claim 1, wherein the ion implantation process is performed in one time without tilt angle.

25. (new) The method of claim 8, wherein the ion implantation process is performed in one time without tilt angle.